

IN THE SPECIFICATION

Page 9, line 17:

One embodiment of a multilayered power supply line employed in a semiconductor integrated circuit, according to the present invention will next be explained in detail with reference to the accompanying drawings. The multilayered power supply line 10 according to the present embodiment can be applied to both a VDD power supply line for supplying a power supply or source potential and a GND power supply line for supplying a ground potential. The VDD power supply line and the GND power supply line to which the multilayered power supply line 10 is applied, may be wired so as to surround the periphery of a block cell 30 as shown in Fig. 3, for example or may be wired as shown in Fig. 4, 5 or 6. Part of the VDD power supply line shown in Fig. 3 is shown in an enlarged form, and a sectional view across the length of the VDD power supply line shown in Fig. 1, which is taken along a dotted line 50, is shown in Fig. 2.

Page 18, between lines 4 and 5, insert new paragraph as follows:

It is to be noted that Figs. 1 and 2 show that the first metal layer (strip) 12, the second metal layer (strip) 14, and the third metal layer (strip) 16 are all lengthwise mutually parallel.
Fig. 1 also shows that the first metal layer 12 and the second metal layer 14 are identical in wiring width, while the third metal layer 16 is narrower (Fig. 7 shows this feature also). Fig. 12 illustrates that pairs of metal strips (e.g., 108 and 102); or, 132 and 142; or, 134 and 144) form a generally planar layer consisting of those strips; and that the source potential V and the ground potential G alternate in adjacent strips of the first metal strip and the third metal strip, and the potential is similar in adjacent strips of the first metal strip and the second metal strip. Fig. 12 also shows that the plurality of strips are arranged in a rectangular array, while Fig. 13 shows that they are mutually parallel.